IDEC Chip Design Contest

Design of High-Efficiency CMOS Radio-Frequency Rectifier For Wireless Power Transfer Systems

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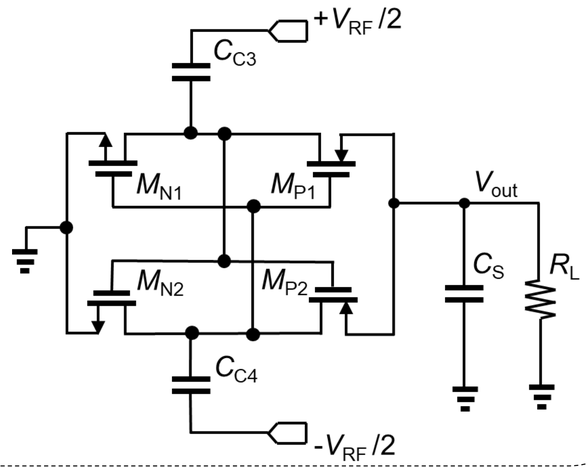
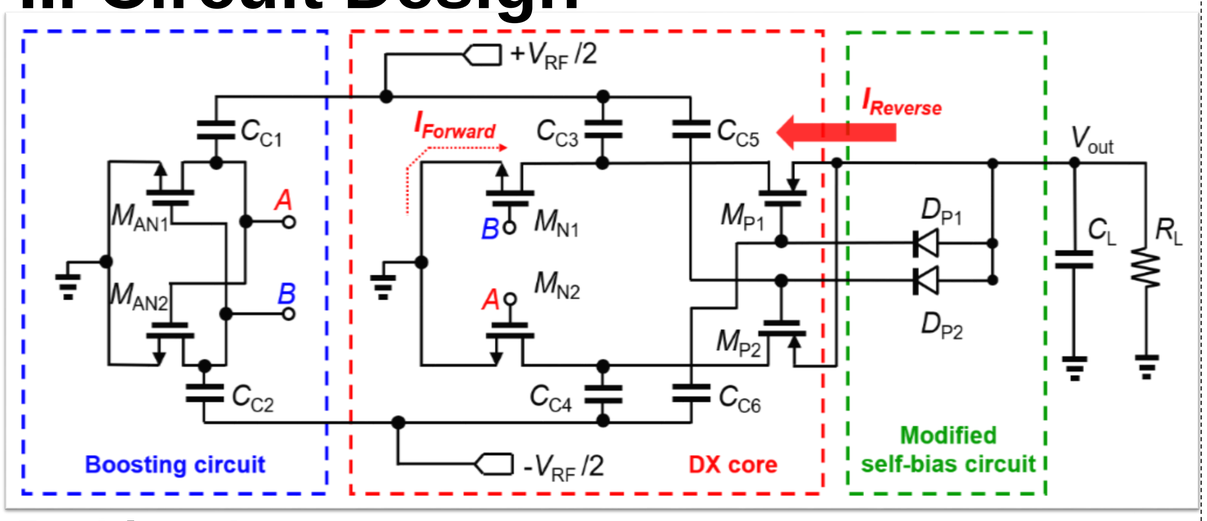
I. Introduction

CMOS Rectifier : Convert AC voltage to DC voltage
Disadvantages of CMOS Rectifier: Low PCE at low and high RF input power.
Solution :
Problems with low RF input power : Add a boosting circuit
Problems with high RF input power : Add a self-biasing circuit

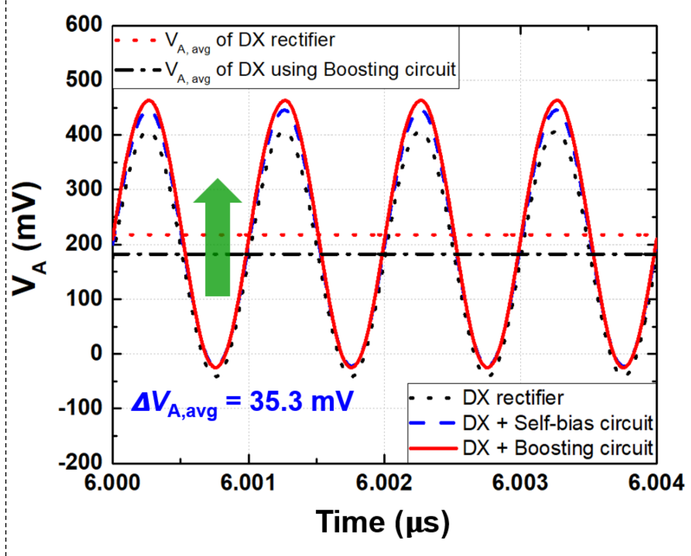


II. Circuit Design



Problem 1: The low turn-on voltage of the CMOS Rectifier's NMOS (M_{N1}, M_{N2}) provides low PCE.

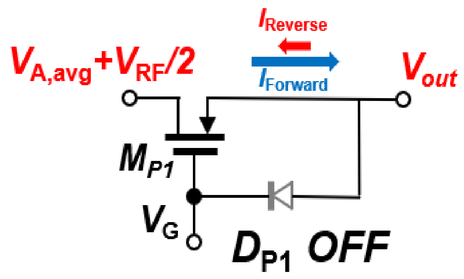
Solution: Minimize power loss by amplifying gate voltage (V_{GS}) of M_{N1} and M_{N2} through boosting circuit to reduce turn-on resistance -> increase PCE.



(Without boosting circuit)
$V_A = V_{RF}/2$,
(With boosting circuit)
$V_A = V_{RF}/2 + V_{A,avg}$

Problem 2: The CMOS rectifier provides a low PCE because the reverse leakage current increases as the gate voltage of the PMOS (M_{P1}, M_{P2}) increases at high RF input power.

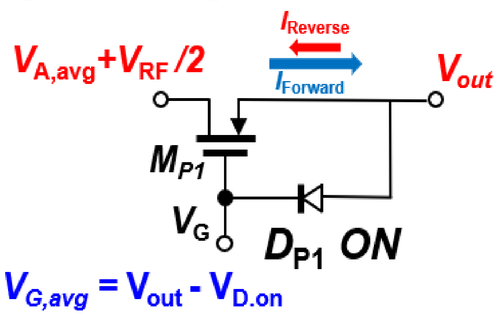
Solution: Reduce the reverse leakage current by adding a self-biasing circuit to lower the gate voltage. -> PCE increase



$V_G = -V_{RF}/2$

V_{SG} (Forward) = $V_{A,avg} + V_{RF}$

V_{SG} (Reverse) = $V_{out} + V_{RF}/2$



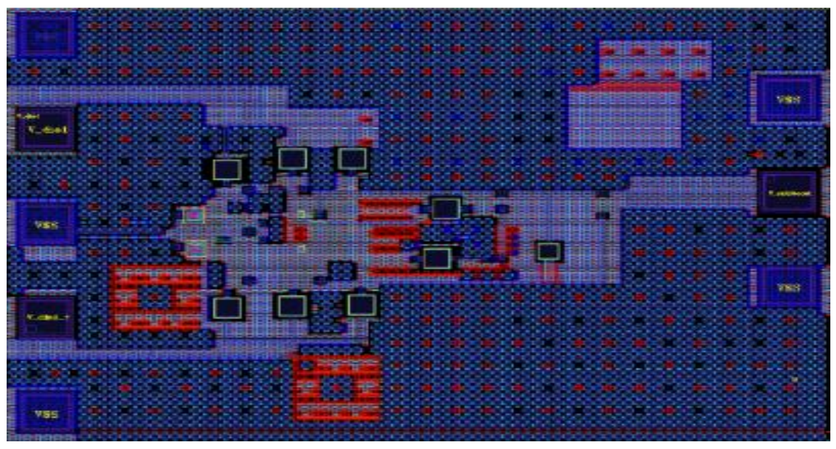
$V_{G,avg} = V_{out} - V_{D.on}$

$V_G = (V_{out}-V_{D.on}) - V_{RF}/2$

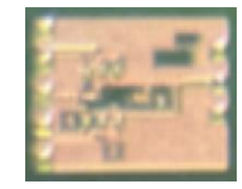
V_{SG} (Forward) = $V_{A,avg} + V_{RF} - V_{G,avg}$

V_{SG} (Reverse) = $V_{D.on} + V_{RF}/2$

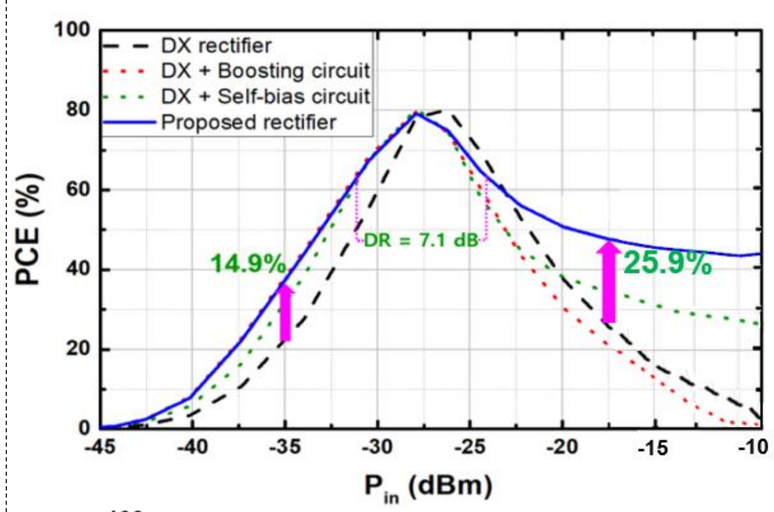
III. Simulation Result



Chip micro graph



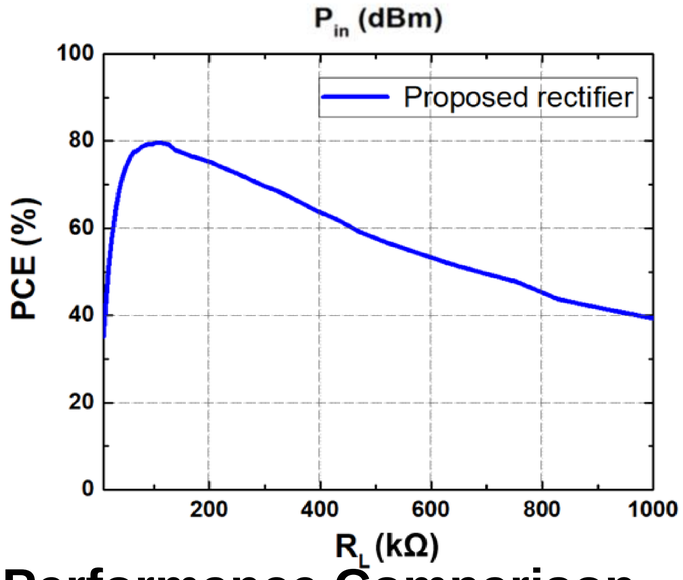
Measurement debugging and analysis in progress



Comparison of PCE between proposed rectifier and CMOS rectifier

Low input power : 14.9% increase

High input power : 25.9% increase



Comparison of PCE according to the size of the load resistance -> Best PCE at 100kΩ

Performance Comparison

Parameter	This Work*	[4]	[8]	[9]	[14]
Technology (μm)	0.18	0.18	0.18	0.18	0.18
Frequency (Hz)	1G	915M	953M	900M	953M
R_L (Ω)	100k	5k	10k	100k	10k
P_{in} (dBm)	-27	-3.7	-12.5	-19.6	-16.8
Peak PCE (%)	79	72.3	67.5	66	70
DR (dB)	7.1	11	4.8	6.4	6.5
Topology	BS	BB	DD	DD	DTR

Acknowledgment

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